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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/033,406	12/26/2001	Kevin X. Zhang	P11680	8560

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EXAMINER	
PATEL, NITIN C	

ART UNIT	PAPER NUMBER
2116	

DATE MAILED: 12/23/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/033,406	ZHANG ET AL.	
	Examiner	Art Unit	
	Nitin C. Patel	2116	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 November 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-18* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *26 December 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *5/10/04, 09/13/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This is in responsive to amendment filed on 16 November 2004.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 1 – 2, 5, 7 – 8, 11 – 12, 16, and 17 – 18, are rejected under 35 U.S.C. 102(e) as being clearly anticipated by Smit et al. [hereinafter as Smit], US Patent 6,446,212 B1.

4. As to claim 1, Smit discloses a processor [10, fig. 1] comprising:

a. a plurality of circuit-blocks [12, processing unit, 26, I/O ports];

b. a plurality of local voltage regulators [14, core regulator, 24, I/O regulator] to each independently provide a local supply voltage to one of the plurality of circuit blocks [12, processing unit, 26, I/O ports], each of the plurality of local voltage regulator [14, 24] being co-located with the circuit block [12, 26] powered by the respective local supply voltage [Vcore, VI/O]; and

c. a global power grid [VDD] to power each of the plurality of local voltage regulator [14, 24] with the global supply voltage [VDD][col. 2, lines 33 – 67, col. 3, lines 1 – 37, fig. 1].

5. As to claim 11, Smit discloses a computer system comprising:

a. a discrete voltage regulator to provide a global supply voltage [VDD] [as it discloses a global voltage supply VDD therefore he teaches a discrete voltage regulator for generating VDD]; and

a processor [10] including

b. a plurality of circuit-blocks [12, processing unit, 26, I/O ports];

c. a plurality of local voltage regulators [14, core regulator, 24, I/O regulator] to each independently provide a local supply voltage to one of the plurality of circuit blocks [12, processing unit, 26, I/O ports], each of the plurality of local voltage regulator [14, 24] being co-located with the circuit block [12, 26] powered by the respective local supply voltage [Vcore, VI/O]; and

d. a global power grid [VDD] to power each of the plurality of local voltage regulator [14, 24] with the global supply voltage [VDD][col. 2, lines 33 – 67, col. 3, lines 1 – 37, fig. 1].

6. As to claim 16, Smit discloses a processor [10, fig. 1] and operation method comprising:

a. providing a global supply voltage [VDD] to a plurality of local voltage regulators [14, core regulator, 24, I/O regulator] through a global power grid [fig. 1], each of the plurality of local voltage regulator [14, 24] being co-located with the circuit block [12, 26] powered by the respective local supply voltage [Vcore, VI/O];and

b. independently provide a local supply voltage [Vcore, VI/O] from each of the plurality of local voltage regulator [14, 24] to power a respective one of the plurality of circuit blocks [12, processing unit, 26, I/O ports][col. 2, lines 33 – 67, col. 3, lines 1 – 37, fig. 1].

7. As to claims 2, 12, and 17, Smit discloses that at least one of the local supply voltage [Vcore] is adjustable by the processor [col. 1, lines 55 – 60, col. 3, lines 40 – 45, fig. 1].

8. As to claim 5, Smit discloses a receiving port [18] to receive global supply voltage [VDD, fig. 1] therefore he teaches an external voltage regulator for generating global voltage [VDD] too.

9. As to claims 7, and 8, Smit discloses a digital circuit [10, processor, fig. 1] wherein at least one of the pluralities of circuit blocks includes at least portion of a core of a processor 1[12, processing unit][col. 2, lines 42 – 54].

10. As to claim 18, Smit discloses a processor [10, fig. 1] with processing unit [12], which comprises a floating point unit of processor too, and independently providing the local power supply voltages [from voltage regulator 14, fig. 1].

Claim Rejections - 35 USC § 103

11. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

12. Claims 3, 6, and 13, are rejected under 35 U.S.C. 103(a) as being unpatentable over Smit et al. [hereinafter as Smit], US Patent 6,446,212 B1 as applied to claims 1, 11, and 16 above, and further in view of McLoughlin, US 5,932,987.

13. As to claims 3, and 13, Smit discloses a processor [10, fig. 1] comprising: a plurality of circuit-blocks [12, processing unit, 26, I/O ports]; a plurality of local voltage regulators [14, core regulator, 24, I/O regulator] to each independently provide a local supply voltage to one of the

plurality of circuit blocks [12, processing unit, 26, I/O ports], each of the plurality of local voltage regulator [14, 24] being co-located with the circuit block [12, 26] powered by the respective local supply voltage [Vcore, VI/O]; and a global power grid [VDD] to power each of the plurality of local voltage regulator [14, 24] with the global supply voltage [VDD][col. 2, lines 33 – 67, col. 3, lines 1 – 37, fig. 1].

However Smit's does disclose the plurality of local voltage regulators [14, 24], but does not include a digitized resistor, which is to be set by the processor. In summary, Smit does not teach to use a digitized resistor.

McLoughlin teaches integrated circuit (52, fig. 22 comprises a digitized resistor [52, a digital resistor] set by the processor [with input lines (60) controlled by the microprocessor] and enables microprocessor to control the reference voltage supplied to the DACS [30], which in turn controls the peak output voltage levels of DACS, and to obtain controlled step size with controlled time and smooth transition from zero to operating voltage [col. 5, lines 47 - 49, col. 6, lines 25 – 37] and implemented in integrated circuit [col. 4, lines 46 – 65].

It would have been an obvious to one of ordinary skill in art, having the teachings of Smit and McLoughlin before him at the time the invention was made, to modify the Smit's regulator and control circuit to include a digitized resistor (digital resistor 52) controlled by microprocessor [col. 4, lines 46 - 55, fig. 2] as taught by McLaughlin, in order to control the peak output voltage level and to obtain controlled step size with controlled time and smooth transition from zero to operating voltage [col. 5, lines 47 - 49, col. 6, lines 25 – 37] and implemented in integrated circuit [col. 4, lines 51 – 65].

14. As to claim 6, McLoughlin discloses an op amp (54) [col. 4, lines 46 – 49, fig. 2].

15. Claims 4, 9 - 10, 14, 15, and 18, are rejected under 35 U.S.C. 103(a) as being unpatentable over Smit et al. [hereinafter as Smit], US Patent 6,446,212 B1, as applied to claims 1, 11, and 16 above, and further in view of Yamamotto et al. [hereinafter as Yamamotto], US Patent 5,778,237 [cited by applicant in IDS filed on January 15, 2004].

16. As to claim 4, Smit discloses reduced instruction set computer and a processor [10, fig. 1] comprising: a plurality of circuit-blocks [12, processing unit, 26, I/O ports]; a plurality of local voltage regulators [14, core regulator, 24, I/O regulator] to each independently provide a local supply voltage to one of the plurality of circuit blocks [12, processing unit, 26, I/O ports], each of the plurality of local voltage regulator [14, 24] being co-located with the circuit block [12, 26] powered by the respective local supply voltage [Vcore, VI/O]; and a global power grid [VDD] to power each of the plurality of local voltage regulator [14, 24] with the global supply voltage [VDD][col. 2, lines 33 – 67, col. 3, lines 1 – 37, fig. 1].

However Smit discloses a processor [10, fig. 1] with a processing unit [12], I/O ports [26], VDD, control unit [16], core regulator [14], I/O regulator [24], I/O port [26] but does not teach explicitly circuit block for timing requirement. In summary, Smit does not teach frequency control for timing requirement.

Ynmamotto discloses a single chip microcomputer [1, fig. 1] with method of controlling [changing] clock frequency and operating voltage [internal voltage] with control circuit [130] with changing [switching] frequency of internal clock with first control circuit [131] as per timing requirement [col. 10, lines 48-67, col. 11, lines 1-33, col. 2, lines 43 - 64, col. 2, lines 39 - 48, col. 8, lines 55-67, col. 9, lines 1-16].

It would have been an obvious to one of ordinary skill in art, having the teachings of Smit and Yamamotto before him at the time the invention was made, to modify the Smit's processor circuit [10] to include clock frequency controlling [changing] and operating voltage [internal voltage] with control circuit [130] with changing [switching] frequency of internal clock with first control circuit [131] as per timing requirement [col. 10, lines 48-67, col. 1 1, lines 1-33, col. 2, lines 43 - 64, col. 2, lines 39 - 48, col. 8, lines 55-67, col. 9, lines 1-16] as taught by Yamamotto, in order to have degree of freedom for switching the operation frequency and voltage of circuit module in accordance with processing performance of module and proportion of data processing to be executed, the operation supply voltage and operating frequency of module can be set relatively freely to optimize the power consumption and data processing efficiency [col. 1, lines 43 – 64].

17. As to claims 9 – 10, Yamamoto discloses a digital circuit [a single chip microcomputer 1] includes at least portion of a core of a processor [100, CPU], and a cache memory region [114 voltage setting register, 124 frequency setting register] with direct memory access controller [103, DMAC][fig. 1].

18. As to claim 14, Yamamoto discloses a single chip microcomputer 1 includes at least portion of a core of a processor [100, CPU], and a cache
memory region [114 voltage setting register, 124 frequency setting register] with direct memory access controller [103, DMAC] and is powered by the local Vcc [113, internal voltage] [fig. 1].

19. As to claim 15, Yamamoto discloses a single chip microcomputer system with CPU [100], which inherently teaches graphic controller.

20. As to claim 18, Yamamoto discloses a single chip microcomputer [1] includes powering a floating point unit [101 MULX, 102 DIVU] of processor [l][fig.1].

21. **Examiner's note:** Examiner has cited particular columns and line numbers in the references as applied to the claims above for the convenience of the applicant. Although the specified citations are representative of the teachings of the art and are applied to the specific limitations within the individual claim, other passages and figures may apply as well. It is respectfully requested from the applicant in preparing responses, to fully consider the references in entirety as potentially teaching all or part of the claimed invention, as well as the context of the passage as taught by the prior art or disclosed by the Examiner.

22. Prior Art not relied upon:

Please refer to the references listed in attached PTO-892, which, are not relied upon for claim rejection since these references are relevant to the claimed invention.

23. Applicant's arguments with respect to claims 1 - 18 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after

the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nitin C. Patel whose telephone number is 571-272-3675. The examiner can normally be reached on 7:00am - 5:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lynne H. Browne can be reached on 571-272-3670. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Nitin C. Patel
December 16, 2004

LYNNE H. BROWNE
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